AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A digital high speed programmable delayed locked loop (DLL) comprises:

a zero degree phase shift digital delay line operably coupled to produce, from a clock signal, a zero phase shifted representation of the clock signal;

a plurality of intermediate phase shift digital delay lines, comprising: ~~at least one intermediate phase shift digital delay line operably coupled to produce, from the clock signal, an intermediate phase shifted representation of the clock signal based on an intermediate control signal~~;

a ninety degree phase-shift digital delay line operably coupled to produce, from the clock signal, a ninety degree phase-shifted representation of the clock signal based on an intermediate control signal;

a one hundred and eighty degree phase-shift digital delay line operably coupled to produce, from the clock signal, a one hundred and eighty degree phase-shifted representation of the clock signal based on the intermediate control signal; and

a two hundred and seventy degree phase-shift digital delay line operably coupled to produce, from the clock signal, a two hundred and seventy degree phase-shifted representation of the clock signal based on the intermediate control signal, wherein the two hundred and seventy degree phase-shifted representation of the clock signal corresponds to the intermediate phase-shifted representation of the clock signal;

a three hundred and sixty degree phase shift digital delay line operably coupled to produce, from the clock signal, a three hundred and sixty degree phase shifted representation of the clock signal based on a three hundred and sixty degree control signal; and

digital control module operably coupled to produce the intermediate control signal and the three hundred and sixty degree control signal based a phase difference between the zero phase shifted representation of the clock signal and the three hundred and sixty degree phase shifted representation of the clock signal.

Claims 2. and 3. (Cancelled)

4. (Original) The digital high speed programmable DLL of claim 1, wherein the zero phase shift digital delay line comprises:

an input impedance that substantially matches an input impedance of the at least one intermediate phase shift digital delay line and of the three hundred and sixty degree phase shift digital delay line.

5. (Original) The digital high speed programmable DLL of claim 1, wherein each of the at least one intermediate phase shift digital delay line comprises:

a coarse digital delay line having a plurality of taps to provide a plurality of phase shifted representations of the clock signal;

a coarse multiplexer module operably coupled to output one of the plurality of phase shifted representations of the clock signal based on the intermediate control signal to produce a selected phase shifted representation of the clock signal;

fine digital delay line having a plurality of fine taps to provide a plurality of phase shifted representations of the selected phase shifted representation of the clock signal; and

a fine multiplexer module operably coupled to output one of the plurality of phase shifted representations of the selected phase shifted representation based on the intermediate control signal to produce the intermediate phase shifted representation of the clock signal.

6. (Original) The digital high speed programmable DLL of claim 1, wherein the three hundred and sixty degree phase shift digital delay line comprises:

a coarse digital delay line having a plurality of taps to provide a plurality of phase shifted representations of the clock signal;

a coarse multiplexer module operably coupled to output one of the plurality of phase shifted representations of the clock signal based on the three hundred and sixty degree control signal to produce a selected phase shifted representation of the clock signal;

fine digital delay line having a plurality of fine taps to provide a plurality of phase shifted representations of the selected phase shifted representation of the clock signal; and

a fine multiplexer module operably coupled to output one of the plurality of phase shifted representations of the selected phase shifted representation based on the three hundred and sixty degree control signal to produce the three hundred and sixty degree phase shifted representation of the clock signal.

7. (Currently Amended) The digital high speed programmable DLL of claim 1, wherein the zero degree phase shift digital delay line comprises:

~~a coarse multiplexer module operably coupled to output the zero phase shifted representation of the clock signal;~~

fine digital delay line having a plurality of fine taps to provide a plurality of phase shifted representations of the zero phase shifted representation of the clock signal, wherein the plurality of phase shifted representations of the zero phase shifted representation of the clock signal includes the zero phase shifted representation of the clock signal;[[and]]

a coarse multiplexer module operably coupled to the input of the fine digital delay line and enabled to output the zero phase shifted representation of the clock signal; and

a fine multiplexer module operably coupled to receive the plurality of the phase shifted representations of the zero phase shifted representation of the clock signal and to output the zero phase shifted representation of the clock signal.

8. (Original) A digital high speed programmable delayed locked loop (DLL) comprises:

a zero degree phase shift digital delay line operably coupled to produce, from a clock signal, a zero phase shifted representation of the clock signal;

a first multiplexer operably coupled to output the zero phase shifted representation of the clock signal or the clock signal based on a mode of operation control signal to produce a first selected clock signal;

at least one intermediate phase shift digital delay line operably coupled to produce an intermediate phase shifted representation of the first selected clock signal based on an intermediate control signal;

a second multiplexer operably coupled to output the intermediate phase shifted representation of the clock signal or the clock signal based on the mode of operation control signal to produce a second selected clock signal;

a three hundred and sixty degree phase shift digital delay line operably coupled to produce three hundred and sixty degree phase shifted representation of the second selected clock signal based on a three hundred and sixty degree control signal; and

digital control module operably coupled to produce the intermediate control signal and the three hundred and sixty degree control signal based a phase difference between the zero phase shifted representation of the clock signal and the three hundred and sixty degree phase shifted representation of the clock signal.

9. (Original) The digital high speed programmable DLL of claim 8, wherein the at least one intermediate phase shift digital delay line comprises:

a plurality of intermediate phase shift digital delay lines.

10. (Original) The digital high speed programmable DLL of claim 9, wherein the plurality of intermediate phase shift digital delay lines comprises:

a ninety degree phase shift digital delay line operably coupled to produce a ninety degree phase shifted representation of the first selected clock signal based on the intermediate control signal;

a third multiplexer operably coupled to output the ninety degree phase shifted representation of the first selected clock signal or the clock signal based on the mode of operation control signal to produce a third selected clock signal;

a one hundred and eighty degree phase shift digital delay line operably coupled to produce a one hundred and eighty degree phase shifted representation of the third selected clock signal based on the intermediate control signal;

a fourth multiplexer operably coupled to output the one hundred and eighty degree phase shifted representation of the third selected clock signal or the clock

signal based on the mode of operation control signal to produce a fourth selected clock signal; and

a two hundred and seventy degree phase shift digital delay line operably coupled to produce a two hundred and seventy degree phase shifted representation of the fourth selected clock signal based on the intermediate control signal, wherein the two hundred and seventy degree phase shifted representation of the fourth selected clock signal corresponds to the intermediate phase shifted representation of the first selected clock signal.

11. (Original) The digital high speed programmable DLL of claim 8, wherein the zero phase shift digital delay line comprises:

an input impedance that substantially matches an input impedance of the at least one intermediate phase shift digital delay line and of the three hundred and sixty degree phase shift digital delay line.

12. (Original) The digital high speed programmable DLL of claim 8, wherein each of the at least one intermediate phase shift digital delay line comprises:

a coarse digital delay line having a plurality of taps to provide a plurality of phase shifted representations of the first selected clock signal;

a coarse multiplexer module operably coupled to output one of the plurality of phase shifted representations of the first selected clock signal based on the intermediate control signal to produce a selected phase shifted representation of the first selected clock signal;

fine digital delay line having a plurality of fine taps to provide a plurality of phase shifted representations of the selected phase shifted representation of the first selected clock signal; and

a fine multiplexer module operably coupled to output one of the plurality of phase shifted representations of the selected phase shifted representation based on the intermediate control signal to produce the intermediate phase shifted representation of the first selected clock signal.

13. (Original) The digital high speed programmable DLL of claim 8, wherein the three hundred and sixty degree phase shift digital delay line comprises:

a coarse digital delay line having a plurality of taps to provide a plurality of phase shifted representations of the second selected clock signal;

a coarse multiplexer module operably coupled to output one of the plurality of phase shifted representations of the second selected clock signal based on the three hundred and sixty degree control signal to produce a selected phase shifted representation of the second selected clock signal;

fine digital delay line having a plurality of fine taps to provide a plurality of phase shifted representations of the selected phase shifted representation of the second selected clock signal; and

a fine multiplexer module operably coupled to output one of the plurality of phase shifted representations of the selected phase shifted representation based on the three hundred and sixty degree control signal to produce the three hundred and sixty degree phase shifted representation of the second selected clock signal.

14. (Original) The digital high speed programmable DLL of claim 8, wherein the zero degree phase shift digital delay line comprises:

a coarse multiplexer module operably coupled to output the zero phase shifted representation of the clock signal;

fine digital delay line having a plurality of fine taps to provide a plurality of phase shifted representations of the zero phase shifted representation of the clock signal, wherein the plurality of phase shifted representations of the zero phase shifted representation of the clock signal includes the zero phase shifted representation of the clock signal; and

a fine multiplexer module operably coupled to receive the plurality of the phase shifted representations of the zero phase shifted representation of the clock signal and to output the zero phase shifted representation of the clock signal.

15. (Currently Amended) A programmable logic device comprises:

an input/output section that includes a digital clock management module;

memory operably coupled to the input/output section; and

programmable logic fabric operably coupled to the memory and the input/output section, wherein the digital clock management module includes a digital high speed programmable delayed locked loop (DLL) that includes:

a zero degree phase shift digital delay line operably coupled to produce, from a clock signal, a zero phase shifted representation of the clock signal;

~~at least one~~ a plurality of intermediate phase shift digital delay lines, comprising: ~~operably coupled to produce, from the clock signal, an intermediate phase-shifted representation of the clock signal based on an intermediate control signal,~~;

a ninety degree phase-shift digital delay line operably coupled to produce, from the clock signal, a ninety degree phase-shifted representation of the clock signal based on the intermediate control signal;

a one hundred and eighty degree phase-shift digital delay line operably coupled to produce, from the clock signal, a one hundred and eighty degree phase-shifted representation of the clock signal based on the intermediate control signal;

a two hundred and seventy degree phase-shift digital delay line operably coupled to produce, from the clock signal, a two hundred and seventy degree phase-shifted representation of the clock signal based on the intermediate control signal, wherein the two hundred and seventy degree phase-shifted representation of the clock signal corresponds to the intermediate phase shifted representation of the clock signal;

a three hundred and sixty degree phase shift digital delay line operably coupled to produce, from the clock signal, a three hundred and sixty degree phase shifted representation of the clock signal based on a three hundred and sixty degree control signal; and

digital control module operably coupled to produce the intermediate control signal and the three hundred and sixty degree control signal based a

phase difference between the zero phase shifted representation of the clock signal and the three hundred and sixty degree phase shifted representation of the clock signal.

Claims 16 and 17. (Cancelled) .

18. (Currently Amended) The programmable logic devices of claim 15, wherein the zero phase shift digital delay line comprises:

an input impedance that substantially matches an input impedance of the ~~at least one intermediate phase shift digital delay line and of the~~ three hundred and sixty degree phase shift digital delay line.

19. (Currently Amended) The programmable logic devices of claim 15, wherein each ~~of the at least one~~ intermediate phase shift digital delay line of the plurality of intermediate phase shift digital delay lines comprises:

a coarse digital delay line having a plurality of taps to provide a plurality of phase shifted representations of the clock signal;

a coarse multiplexer module operably coupled to output one of the plurality of phase shifted representations of the clock signal based on the intermediate control signal to produce a selected phase shifted representation of the clock signal;

fine digital delay line having a plurality of fine taps to provide a plurality of phase shifted representations of the selected phase shifted representation of the clock signal; and

a fine multiplexer module operably coupled to output one of the plurality of phase shifted representations of the selected phase shifted representation based on the intermediate control signal to produce the intermediate phase shifted representation of the clock signal.

20. (Original) The programmable logic devices of claim 15, wherein the three hundred and sixty degree phase shift digital delay line comprises:

a coarse digital delay line having a plurality of taps to provide a plurality of phase shifted representations of the clock signal;

a coarse multiplexer module operably coupled to output one of the plurality of phase shifted representations of the clock signal based on the three hundred and sixty degree control signal to produce a selected phase shifted representation of the clock signal;

fine digital delay line having a plurality of fine taps to provide a plurality of phase shifted representations of the selected phase shifted representation of the clock signal; and

a fine multiplexer module operably coupled to output one of the plurality of phase shifted representations of the selected phase shifted representation based on the three hundred and sixty degree control signal to produce the three hundred and sixty degree phase shifted representation of the clock signal.

21. (Currently Amended) The programmable logic devices of claim 15, wherein the zero degree phase shift digital delay line comprises:

~~a coarse multiplexer module operably coupled to output the zero phase shifted representation of the clock signal;~~

fine digital delay line having a plurality of fine taps to provide a plurality of phase shifted representations of the zero phase shifted representation of the clock signal, wherein the plurality of phase shifted representations of the zero phase shifted representation of the clock signal includes the zero phase shifted representation of the clock signal;[[and]]

a coarse multiplexer module operably coupled to the input of the fine digital delay line and enabled to output the zero phase shifted representation of the clock signal; and

a fine multiplexer module operably coupled to receive the plurality of the phase shifted representations of the zero phase shifted representation of the clock signal and to output the zero phase shifted representation of the clock signal.

22. (Original) The programmable logic devices of claim 15, wherein the digital high speed programmable DLL further comprises:

a plurality of multiplexers operably coupled to configure the zero degree phase shift digital delay line, the at least one intermediate phase shift digital delay line, and the three hundred and sixty degree phase shift digital delay line in parallel manner for high speed operations and in a serial manner for lower speed operations.